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High Speed Computerized Data Acquisition of Photovoltaic V-I Characteristics

Richard DeLombard and Ronald C. Cull
National Aeronautics and Space Administration
Lewis Research Center

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HIGH SPEED COMPUTERIZED DATA ACQUISITION OF PHOTOVOLTAIC V-I CHARACTERISTICS

by Richard DeLombard and Ronald C. Cull

NASA Lewis Research Center
Cleveland, Ohio

E-1387

A. INTRODUCTION

The NASA Lewis Research Center is operating the National Photovoltaic Systems Test Facility (STF) at Cleveland, Ohio, for the Department of Energy as part of the National Photovoltaic Energy Program. A continuing task in facility operations is the acquisition of the voltage-current (V-I) characteristics of the photovoltaic array under actual environmental conditions. Operational goals of the STF include operational ease and speed of data acquisition, data accuracy and automated V-I data acquisition from the 300 individual strings of the STF array. Previous methods used in the STF for V-I characteristic data acquisition have had disadvantages with respect to the goals of STF operations. Single data point acquisition was extremely slow and the V-I measurements were susceptible to varying insolation and thermal conditions. Recording V-I characteristics with an analog X-Y plotter in real time yields an increase in speed but data which is difficult to analyze numerically and still susceptible to variability in insolation and thermal conditions.

To alleviate these deficiencies and to provide for V-I data corrected to standard conditions of insolation and temperature, a new method of data acquisition was devised. This new method uses a capacitor charge technique to obtain the V-I characteristic and a computerized data system to display, record and process the data. This method yields an overall system that satisfies the STF goals of data acquisition speed, accuracy and ease of operation. This method is explained in section B, the STF system using this method is explained in section C, and typical data displays are presented in section D.

B. METHOD OF OBTAINING V-I CHARACTERISTICS

The capacitor charge technique uses an array shorting switch and a capacitor bank to sweep the array operating voltage and current from short circuit to open circuit in a specified time. In the basic configuration, Figure 1(a), the array segment, the shorting switch and the capacitor bank are connected in parallel. The array segment is first shorted by closing the switch, to put the array segment at the short circuit operating point. The switch is opened to initiate the V-I process. The relatively constant array current from the short circuit condition to the maximum power point charges the capacitor so that the voltage increases approximately linearly with time. Past the maximum power point, the array current and the charging rate decrease as the array segment operating point approaches an open circuit condition asymptotically. A data acquisition system repetitively samples the array voltage and current during the sweep from short circuit to open circuit.

Although this method produces a V-I curve in only the fourth quadrant, it is possible, if desired, to force the V-I operating point into the first and third quadrants. A current-regulated voltage-limited power supply, I_S in

Fig. 1(b), may be added in series with the PV array to reverse the array voltage into the third quandrant and increase the array current past the short circuit point. This method enables the investigation of the V-I characteristics around the short circuit point and the reverse breakdown characteristics. A voltage-regulated current-limited power supply, V_S in Fig. 1(b), may be added in parallel with the PV array to increase the voltage of the array beyond the open-circuit point and reverse the array current into the first quadrant. This enables the investigation of the V-I characteristics around the open circuit point.

C. SYSTEM DESCRIPTION

The STF system for V-I data acquisition consists of the computerized data system (CDS), a synchronization panel, array shorting transistors, a variable capacitor bank and a variable resistive load bank. (Figure 2) The system is capable of acquiring fourth quadrant V-I data on PV array segments ranging in size from 20 Wp to 15 kWp and having a maximum open circuit voltage of 300 volts and a maximum short circuit current of 100 amps.

The CDS consists of a microprocessor based data acquisition computer located in the STF, and a minicomputer and data collector located in the LeRC central computer facility, the Research Analysis Center (RAC). The array transition from short circuit to open circuit is synchronized with the data acquisition by the synchronization panel. This extensive CDS equipment may be simplified for field use by incorporating a mass storage device with a data acquisition computer.

The timing diagram is shown in Figure 3. The process is started at t_1, by the operator pressing either of the RESET switches. This initiates a sequence that pre-loads the array and discharges the capacitors by connecting the resistive load bank on the bus. When the array voltage becomes less than approximately 40 volts, the shorting transistor is switched on, t_2. The isolation diode, D_1, protects the shorting transistors and the wiring from high currents associated with non-current-limited sources (i.e. batteries, capacitors) that may be connected to the bus. There is a time period during which the resistive load bank and the shorting transistor are both on. This is to ensure that the array remains loaded at the time the shorting transistors are turned on and also to allow the capacitors to discharge further after the shorting transistors are turned on. When the resistive load bank is removed from the bus, t_3, the system is ready to acquire data for a V-I curve of the connected array segment. To minimize arcing, manual switching of capacitors to select the proper capacitance size is done when the capacitors are discharged and the bus voltage is essentially zero.

To initiate the acquisition of the V-I characteristics, the operator presses the INITIATE V-I pushbutton. The CDS detects the switch closure and signals the synchronization panel to turn the shorting transistors off, t_4, which starts the array sweep from short circuit to open circuit. The CDS delays the initiation of data acquisition for a short period of time to allow for relay switching delays.

The CDS samples 105 pairs of voltage and current data and 25 channels of facility data during the data acquisition time frame which is fixed at 125 milliseconds.

The time required for the array to sweep from short circuit to open circuit must be matched to the data acquisition time frame of the CDS. This array sweep time is set by the capacitor size, which is a function of array open circuit voltage and array short circuit current. A technique for calculating the required capacitance values for a given array is presented in Appendix 2.

After the data acquisition is completed, the CDS displays the facility data on an alphanumeric CRT screen (Figure 4) and plots the raw data on a graphics CRT terminal (Figures 5 and 6). These displays are used to visually check the validity of the data before it is transferred to mass storage in the data collector. Problems such as using a capacitor of the wrong size or having additional array sections connected have been detected by these means.

The variable capacitor bank has a total capacitance of 66 760 ufd and is switchable in units as small as 50 ufd. Table 1 lists the major characteristics of the capacitor bank.

The transistors used to short the array have a safe operating area (SOA) characteristic that limits the applied voltage to the transistors to 40 volts at the maximum array current. A meter relay is used in the circuit to allow the transistors to turn on only if the applied voltage is less than 40 volts. Since the meter must also display the array voltage ranging up to 300 volts, and must accurately sense the 40 volt level, a non-linear meter relay circuit was used. A description of the circuit is presented in Appendix 1.

D. DATA

The data that is available is raw voltage-current data, ambient facility data, voltage-current data corrected to standard operating conditions (SOC) and graphic plots. The SOC are defined to be an insolation level of 100 mW/cm^2 and a cell junction temperature of 28° C.

The data is available in facility alphanumeric CRT displays, facility graphics CRT displays and RAC processed data.

The facility alphanumeric CRT display for a V-I curve is shown in Figure 4. The facility data for V-I measurements is ambient insolation, module temperatures, ambient temperature, humidity, wind velocity and direction, and array segment identification. This data allows an evaluation of the conditions at the time of the V-I data. This CRT, which is updated approximately every two seconds, displays real time data when V-I data is not being acquired.

Examples of the CRT graphic display of the raw V-I data taken with optimum and non-optimum sweep rates are shown in Figure 5. These illustrate the sweep rate difference for the same array and different capacitor sizes. The plot in Figure 5a has a capacitor that is too large. The sweep rate is low and the array does not reach open circuit before the data acquisition time frame has ended. The plot in Figure 5b has a capacitor that is too small. The sweep rate is high and the data points are spread out too much for accurate analysis of shape, fill factor, etc. The plot in Figure 5c has a capacitor of an optimal value. The data points are sufficiently close for analysis and open circuit is reached at the end of the data acquisition time frame.

Fig. 6 is a V-I plot taken of a 120 volt (nominal) array composed of two current mismatched series sections of 40 volts and 80 volts. The characteristics are accurately reproduced for even this complex array.

Figures 7 through 10 illustrate the processed data available from the RAC. Experimental data is shown as a V-I curve in Figure 7 and as a voltage - power (V-P) curve in Figure 8. Data, corrected to SOC, is shown as a V-I curve in Figure 9 and as a V-P curve in Figure 10. Other data, both measured (e.g. temperature) and calculated (e.g. fill factor) is printed on the plot as well as the identification (configuration number) of the array segment under test.

E. SUMMARY

A photovoltaic V-I data acquisition system has been developed by the LeRC. The system has been used for routine measurement of the STF PV array and has the following demonstrated advantages:

(a) Speed - The time required to acquire data for a single V-I characteristic is approximately five seconds.

(b) Accuracy - The environmental conditions remain essentially constant during the small fraction of a second required for data acquisition. The data has also been compared with data obtained from a flash simulator and single point measurements and is in close agreement.

(c) Real time data observation - The data can be examined for proper timing prior to recording.

(d) Ease of data analysis - The data is acquired, recorded, normalized and plotted by computers with no manual intervention necessary.

(e) Future Automation - This system is compatible with present and future growth of the STF toward fully automated V-I data acquisition.

This system has been installed and operational since June 1979 and has been a major factor in the ongoing array performance and degradation program for the STF PV array.

Appendix 1 Nonlinear Meter Circuit and Characteristics

The capacitor charge technique as installed in the STF requires a meter relay to perform two functions. The meter must display system DC bus voltages up to 300 volts and must also provide a contact closure at 40 volts with a certain degree of accuracy. The 40 volt limit is imposed by the safe operating area of the particular transistor type used as an array shorting transistor.

The circuit in Figure A1-1 was designed and calibrated for use in the system. The 1N3604 diode is used to clamp the maximum voltage seen by the meter relay and the 680 Ω resistor. At the maximum input voltage of 300 volts, the diode voltage is approximately 0.7 volts, biased by the current through the 50K Ω resistor. The 680 Ω resistor and the meter resistance act to divide the 700 mV to 50 mV at the meter. The nonlinear characteristic of the diode introduces a nonlinear characteristic to the meter reading which allows an accurate set point adjustment at 40 volts as well as a full scale range of 300 volts.

The characteristic of this meter circuit is shown in Figure A1-2.

Appendix 2 Capacitance Calculation for Capacitor Charge PV V-I Technique

In the capacitor charge technique, a PV array charges a capacitor from short circuit to open circuit. Coincident with this transition, the voltage and current data are acquired by the CDS in a fixed time frame. These two events must be synchronized for accurate data to be obtained. Since the CDS time frame is fixed by the CDS equipment, a means of adjusting the capacitor charging time is needed.

Three factors have a major effect on the time required for the array to sweep from short circuit to open circuit; the array open circuit voltage, the array short circuit current and the capacitance of the capacitor. For a given array and insolation level, the capacitor size is the only variable available to coordinate the array sweep time and the data acquisition time. The procedure to calculate the required amount of capacitance for a given array configuration is presented here.

A PV array V-I characteristic can be represented as a two step linear approximation, Figure A2-1. For purposes of calculation, an equivalent circuit, Figure A2-2, is used for the sweep from short circuit to the maximum power point. The time required to charge the capacitor from short circuit to the maximum power point, Δt_1, is obtained from the capacitor equation,

$$I = C\ dv/dt$$

With $I = I_{sc}$, $dv \cong \Delta V = V_{mp} - V_{sc} = V_{mp}$

and $dt \cong \Delta t_1$

then $$\Delta t_1 = \frac{V_{mp} C}{I_{sc}}$$

For the transition from the maximum power point to open circuit, an equivalent circuit is shown in Figure A2-3. The capacitor has an initial charge voltage equal to Vmp. The effective resistance is given by

$$R_{eff} = (V_{oc} - V_{mp})/I_{sc}$$

The capacitor voltage now follows the equation

$$V_c = V_{oc} + (V_{mp} - V_{oc})e^{-(t/R_{eff}C)}$$

Since the array operating point approaches the open circuit condition asymptotically, the time required for the capacitor voltage to reach k percent of V_{oc}, Δt_2, is given by

$$\frac{k}{100} V_{oc} = V_{oc} + (V_{mp} - V_{oc})e^{-(\Delta t_2/R_{eff}C)}$$

This reduces to

$$e^{-(\Delta t_2/R_{eff}C)} = \frac{100 - k}{100} \quad \frac{1}{1 - r}$$

where r is a function of the PV characteristics and is defined by

$$r = V_{mp}/V_{oc}.$$

Then

$$\Delta t_2 = \frac{V_{mp} - V_{oc}}{I_{sc}} \; C \; \ln \left[\frac{100 - k}{100} \quad \frac{1}{1 - r} \right]$$

The total time required for the transition from short circuit to k percent of open circuit voltage is

$$t = \Delta t_1 + \Delta t_2 = \frac{V_{mp}C}{I_{sc}} + \frac{V_{mp} - V_{oc}}{I_{sc}} \; C \; \ln \left[\frac{100 - k}{100} \quad \frac{1}{1 - r} \right]$$

then

$$t = \frac{r \, V_{oc}C}{I_{sc}} \left\{ 1 + (1 - \frac{1}{r}) \; \ln \left[\frac{100 - k}{100} \quad \frac{1}{1 - r} \right] \right\}$$

For the STF array we have used a value of 98 percent for k and 0.8 for r. This value for r is a typical value for terrestrial photovoltaic modules. These values then result in

$$T = 1.261 \frac{V_{oc}C}{I_{sc}}$$

With the CDS time frame for data acquisition set at 125 ms, the required capacitor size is given by

$$C = 9.91 \times 10^4 \frac{I_{sc}}{V_{oc}} \mu F$$

This relationship between the array short-circuit current, the array open-circuit voltage, and the required capacitance was used to construct the capacitance calculation chart shown in Figure A2-4. The chart is normalized for 1 ampere of short-circuit current. Since the required capacitance is a linear function of the short-circuit current, the current scale may be changed by a scale factor, which would change the required capacitance by the same factor. For example, consider the data point in Figure A2-4. For an open-circuit voltage of 200 volts and a short-circuit current of 0.5 ampere, the required

capacitance is 250 μF. If the short-circuit current were 5 amperes instead of 0.5 ampere, the required capacitance would be 2500 μF. Again, if the short-circuit current were 50 amperes, the required capacitance would be 25 000 μF. By observing the open-circuit voltage and the short-circuit current during initialization of the system, the operator can select the required capacitance from the chart.

Table I. - Variable Capacitor Bank Characteristics

Maximum voltage	350	VDC
Bleed resistor	10	MΩ/capacitor
Total capacitance	66 760	μF

Capacitance value (μF)	Number of switched steps
2500	24
860	4
420	4
220	4
140	4
50	4

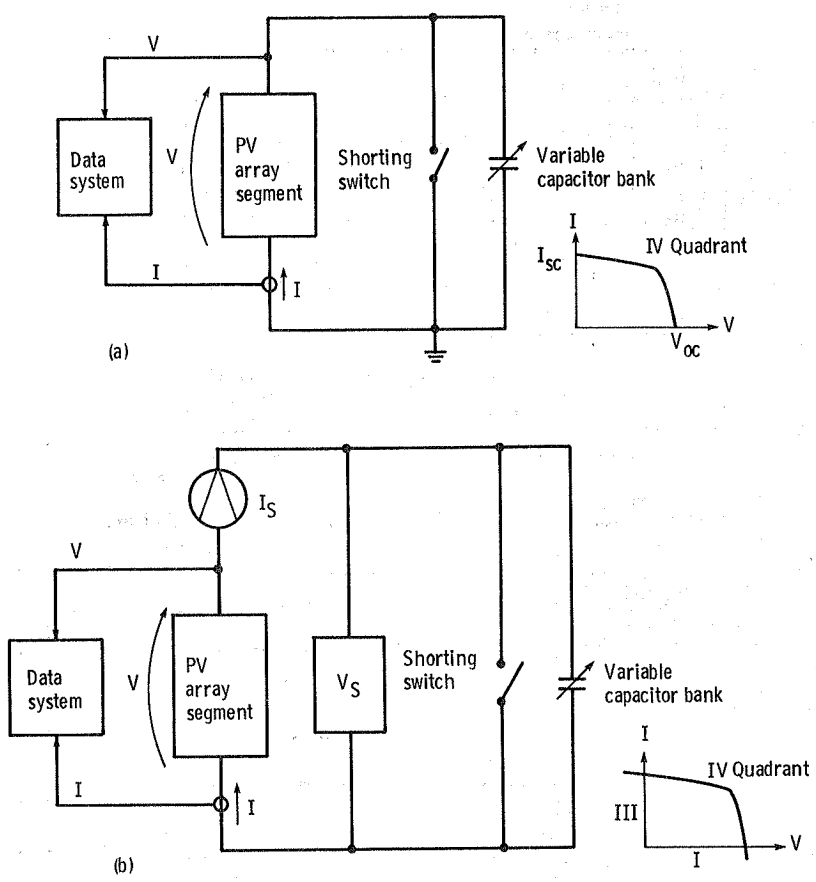

Figure 1. - Fourth quadrant (a) and first, third and fourth quadrant (b) V-I operation.

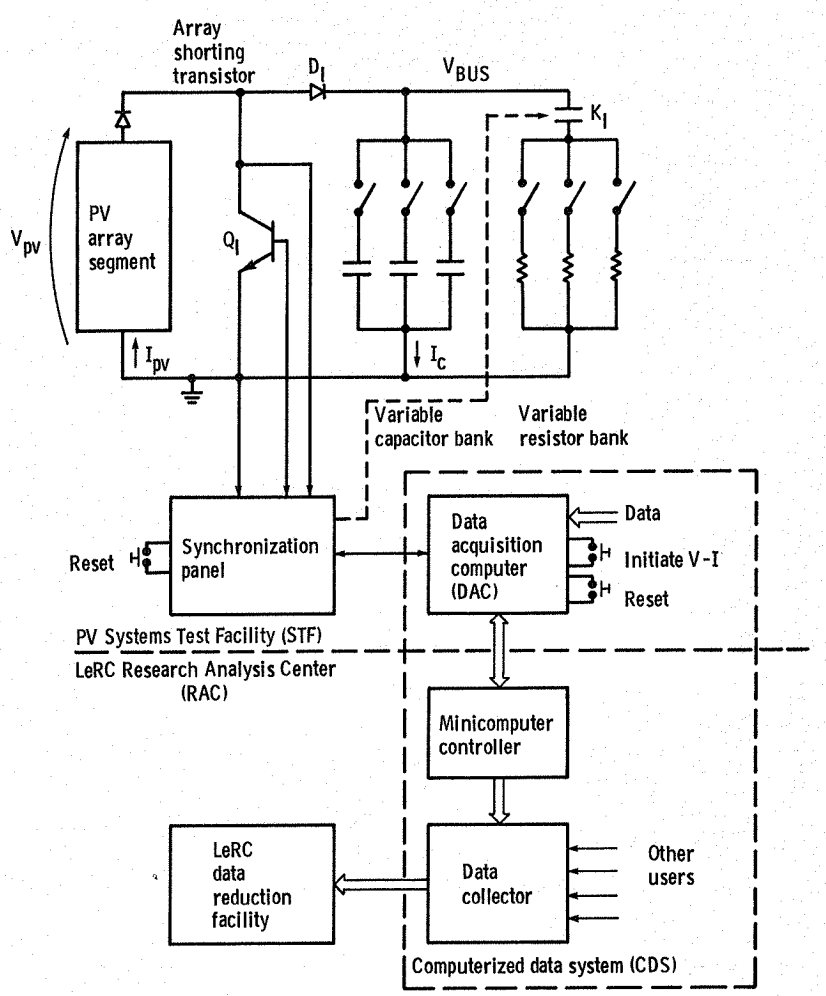

Figure 2. - STF V-I data acquisition system.

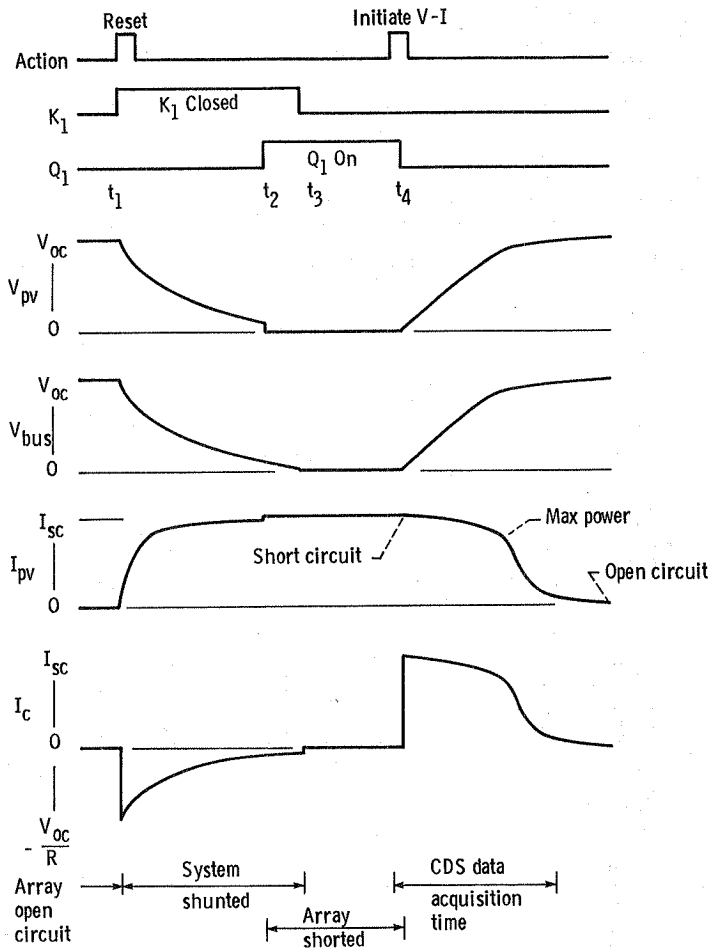

Figure 3. - V-I timing diagram.

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PHOTOVOLTAIC SYSTEM TEST FACILITY

CONFIGURATION 10. I-V SWEEP DELAY 0. 1/60 SECOND TICS

LAST READING NO. 1109.

IF	BLK 1 ROW 10	100.4	MW/CM2
IS	NO GRD REFL	100.1	MW/CM2
IFT	BLK 3 ROW 7	99.8	MW/CM2
IFCT	BLK 3 ROW 5	99.0	MW/CM2
IWT	BLK 3 ROW 7 W	99.5	MW/CM2
IET	BLK 3 ROW 7 E	96.3	MW/CM2
TI	TOT INSOL APPLY	101.8	MW/CM2
IM	STD INSOL WH	639.8	WH/M2
WV	WIND VELOCITY	6.8	MPH
WD	WIND DIRECTION	135.0	DEG
HUMD	REL HUM	40.0	%

AMBT	AMB AIR TEMP	10.0	DEG C
MTSX	MODULE TEMP SX	-126.7	DEG C
MTST	MODULE TEMP ST	26.8	DEG C
MTSP	MODULE TEMP SP	34.1	DEG C
MTSTG	MODULE TEMP STGLAS	133.8	DEG C
MTSTE	MODULE TEMP STTE	24.6	DEG C
MTSTT	MODULE TEMP STT	25.2	DEG C
TRW	TOT ARRAY WATTS	39.8	WATTS
TRV	TOT ARRAY VOLTS	146.13	VOLTS
TRAS	TOTAL ARRAY AMPS	0.71	AMPS
TRA-2	TOTAL ARRAY AMPS	0.24	AMPS

Figure 4. - Facility data display.

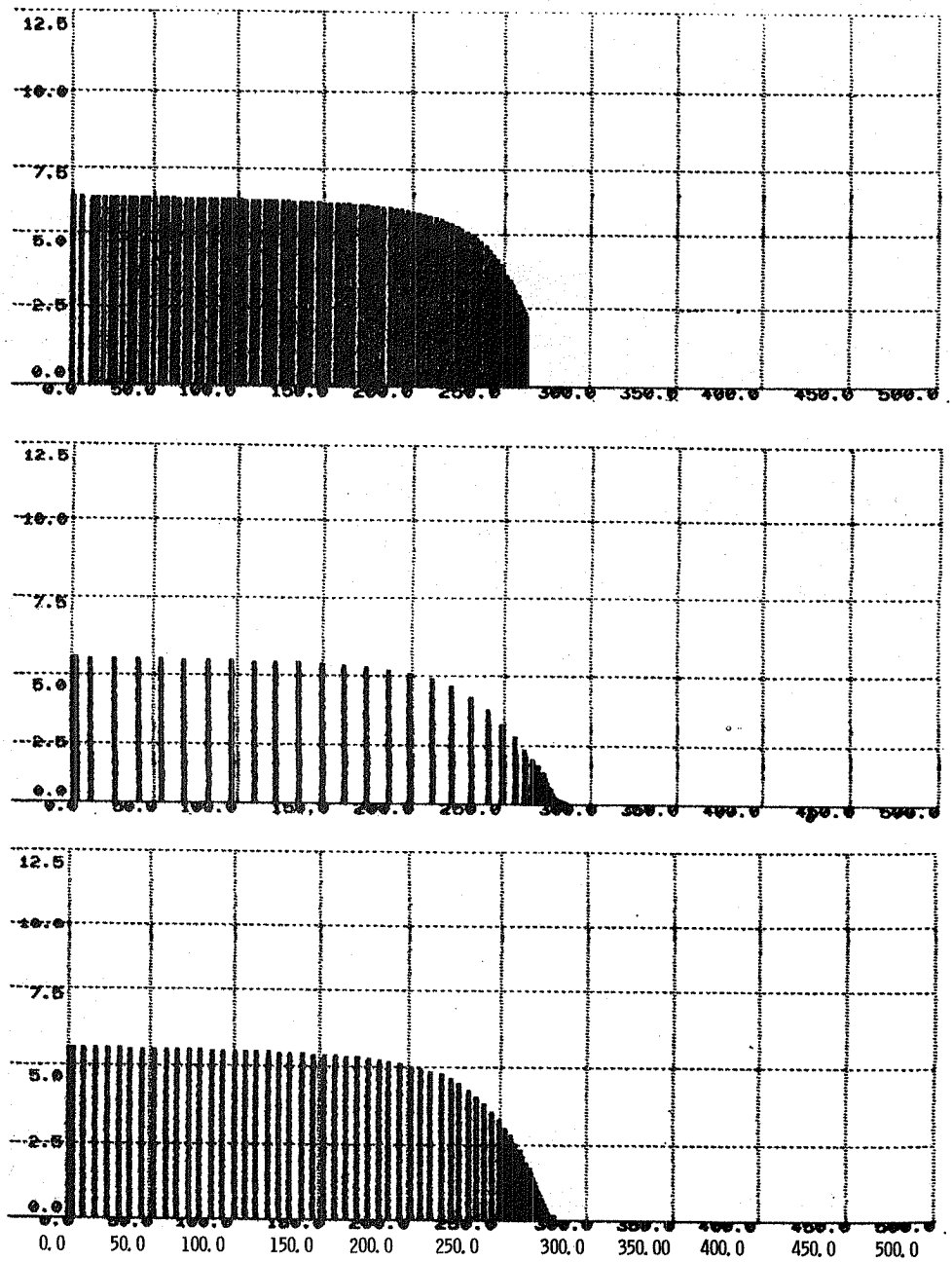

Figure 5. - Raw V-I data display.

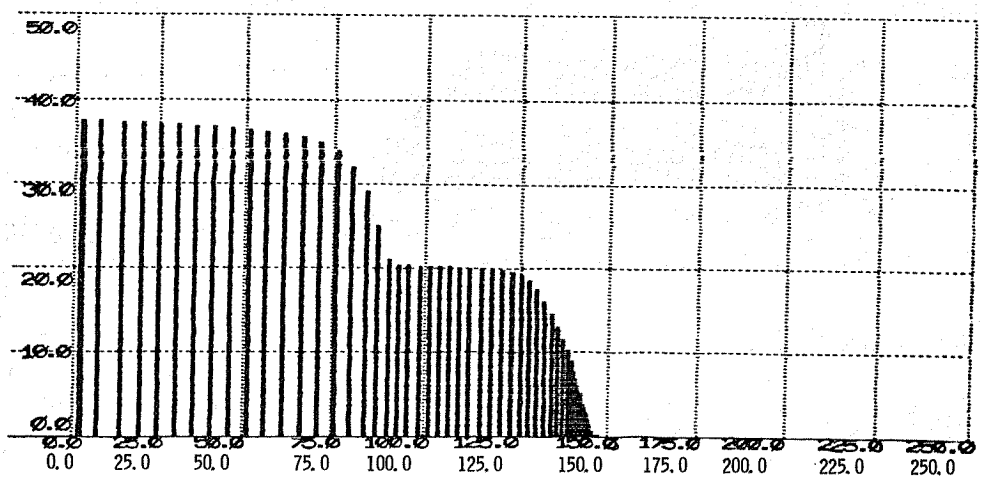

Figure 6. - Raw V-I data display.

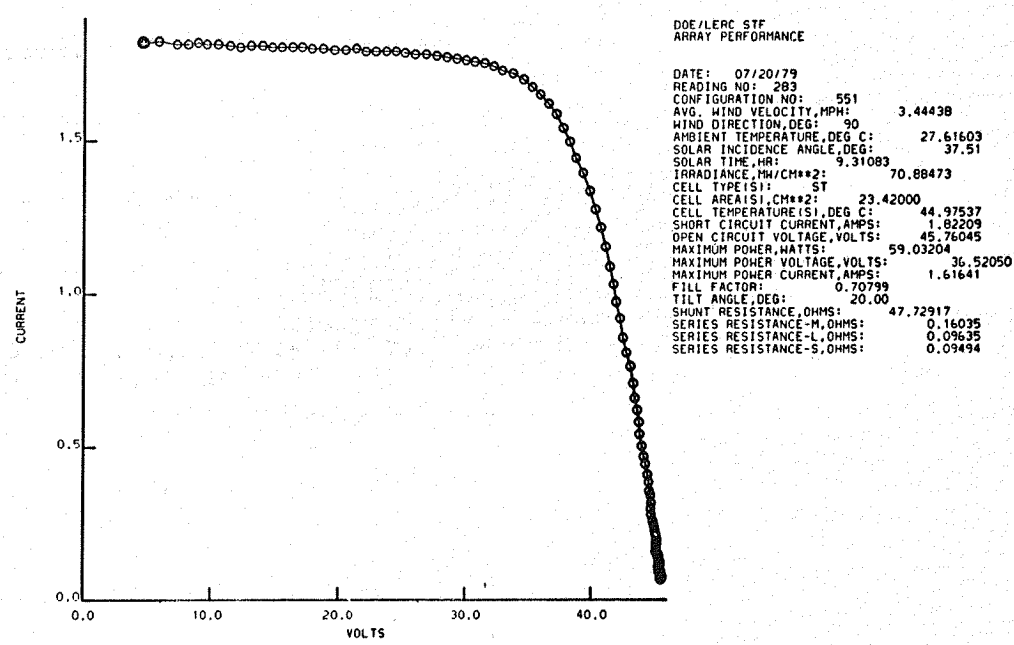

Figure 7. - Experimental data output from computerized data system.

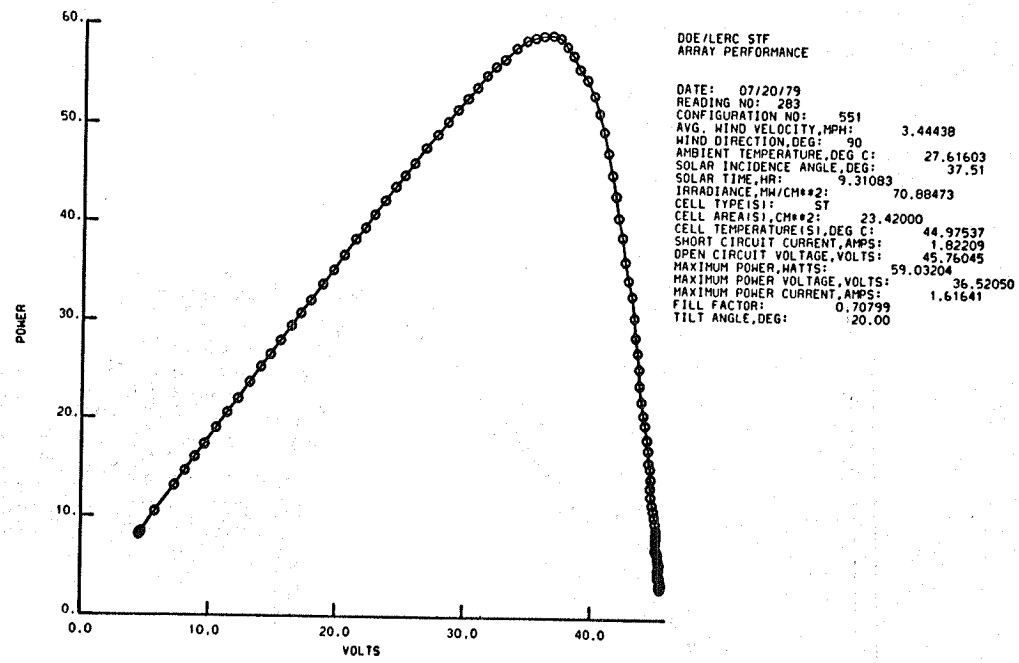

Figure 8. - Experimental data output from computerized data system.

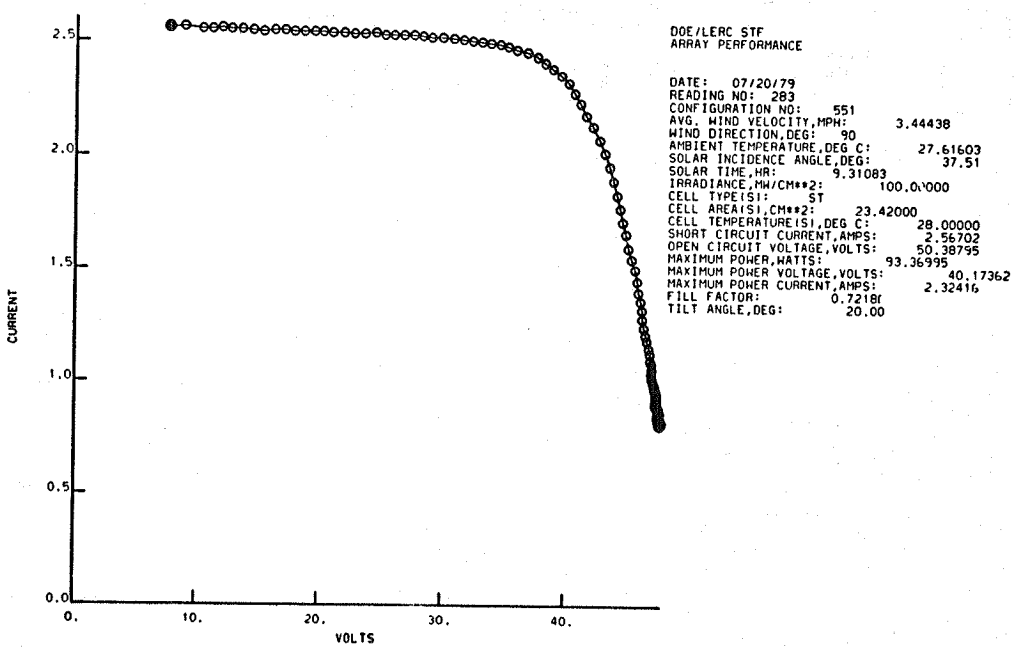

Figure 9. - Data corrected to standard operating conditions (SOC).

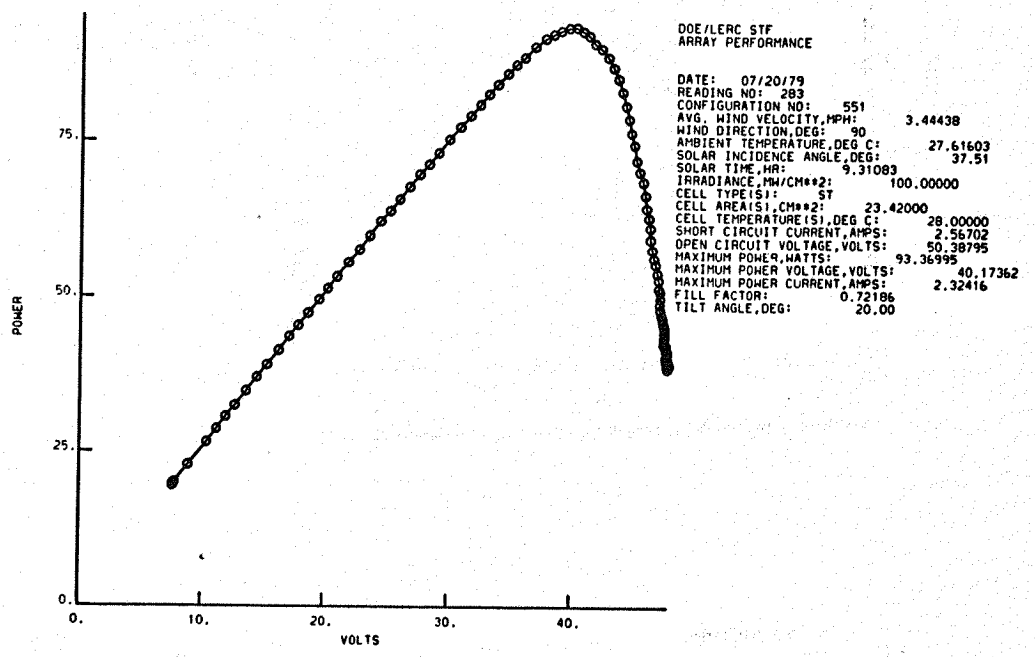

Figure 10. - Data corrected to standard operating conditions (SOC).

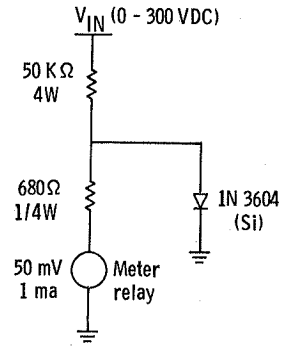

Figure A1-1. - Nonlinear meter circuit.

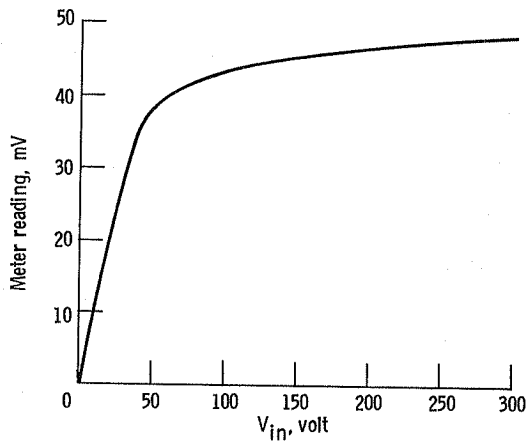

Figure A1-2. - Nonlinear meter circuit characteristic.

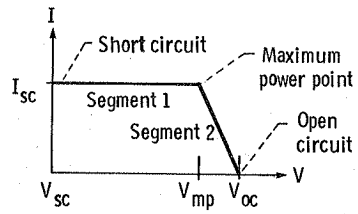

Figure A2-1. - Linear approximation of PV characteristics.

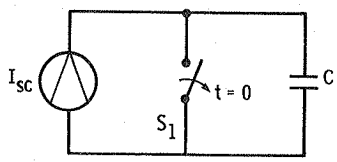

Figure A2-2. - Equivalent circuit for segment 1.

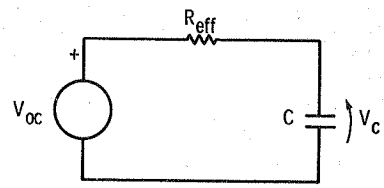

Figure A2-3. - Equivalent circuit for segment 2.

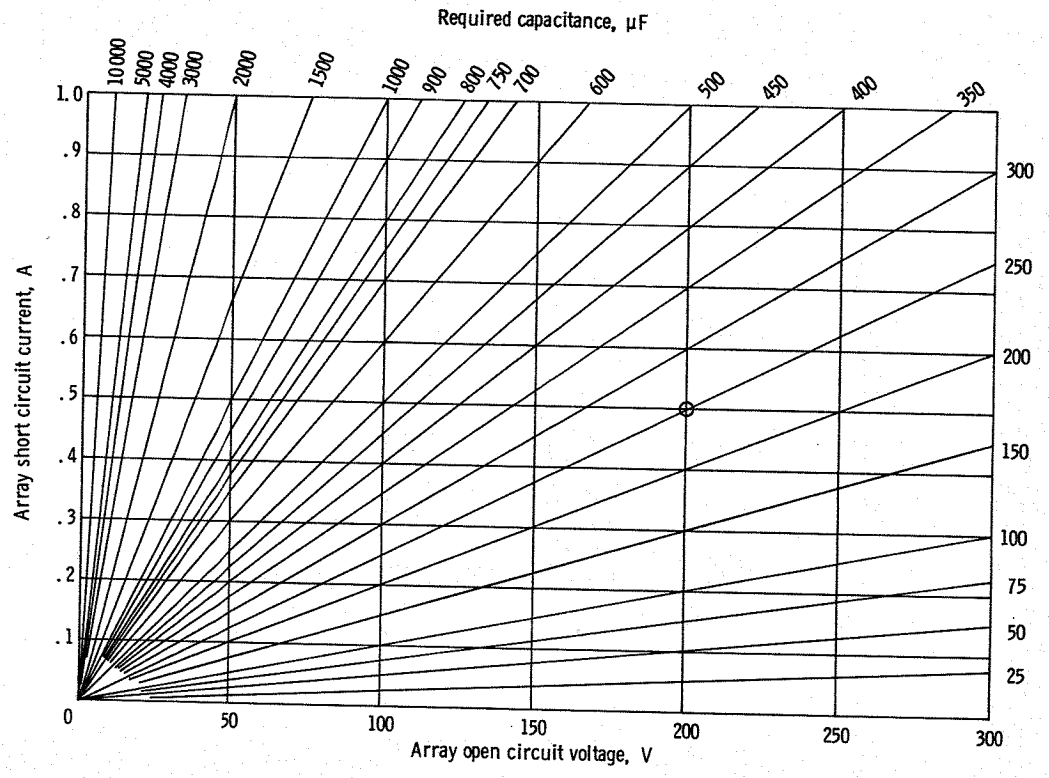

Figure A2-4. - Capacitance calculation chart.

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16. Abstract

The NASA Lewis Research Center is operating the National Photovoltaic Systems Test Facility (STF) at Cleveland, Ohio, for the Department of Energy as part of the National Photovoltaic Energy Program. A continuing task in facility operations is the acquisition of the voltage-current (V-I) characteristics of the photovoltaic array under actual environmental conditions. A method of data acquisition was devised that uses a capacitor charge technique to obtain the V-I characteristic and a computerized data system to display, record and process the data. The capacitor charge technique uses an array shorting transistor and a capacitor bank to sweep the array operating voltage and current from short circuit to open circuit in a specified time (approximately 125 ms). The computerized data system is synchonized with this transition and repetitively samples the array voltage and current during the transition and records the ambient conditions. This data is then normalized by the computer to standard conditions (100 mW/cm^2, 28^{o} C) and is available in tabular and graphic form for both the voltage-current and voltage-power characteristics. The report contains a description of the capacitor charge technique, a description of the system installed in the STF and sample data.

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